VLSI HW3

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1.

Simulate the input capacitance of the first inverter

一張含有 坐, 電腦, 電子用品 的圖片

自動產生的描述

一張含有 螢幕擷取畫面 的圖片

自動產生的描述

The first inverter’s Cin is 3.9284fF

1.(a)

一張含有 文字 的圖片

自動產生的描述

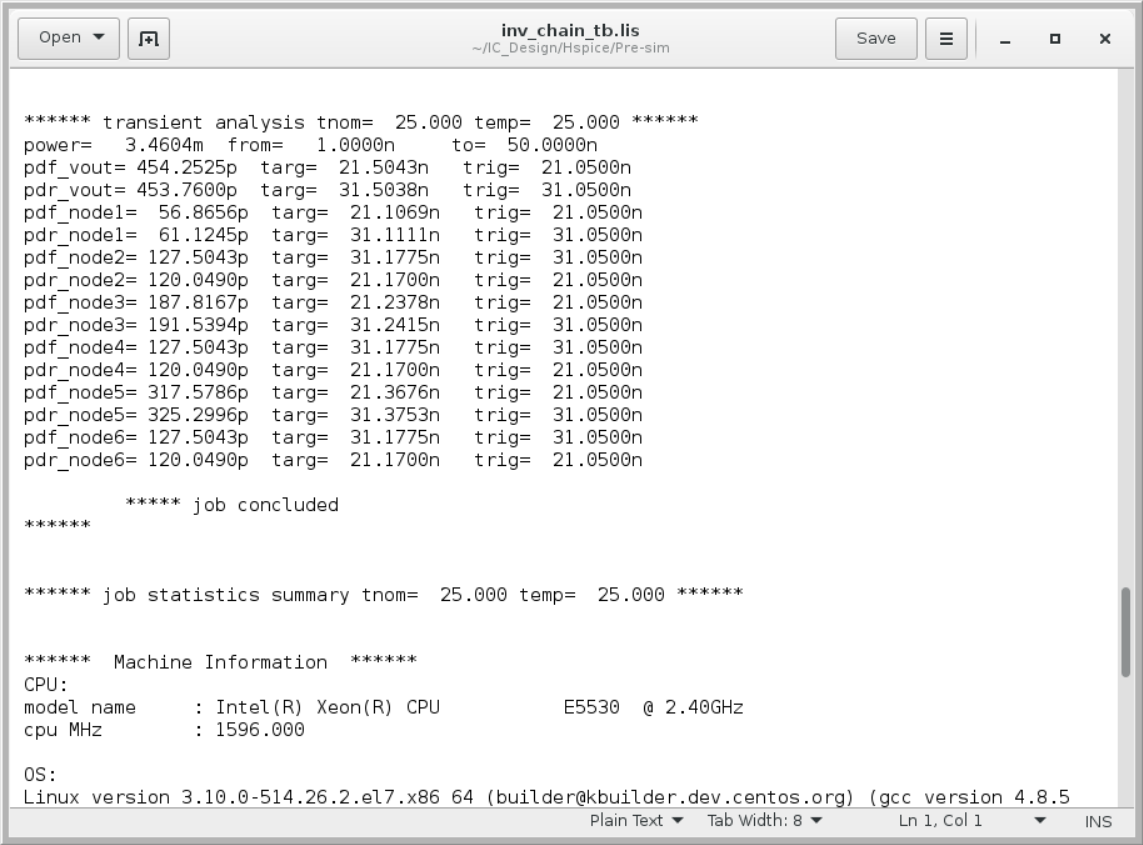
1.(b)

tpdr

tpdf

一張含有 文字 的圖片

自動產生的描述



1.(c)

一張含有 螢幕擷取畫面 的圖片

自動產生的描述

C(total) = Cin + Cout + Cnode1 + … + Cnode6

= 13.9382f + 46.1028f + 128.1861f + 432.6417f + 1.2254p + 4.1346p + 3.9284f + 14.4245p

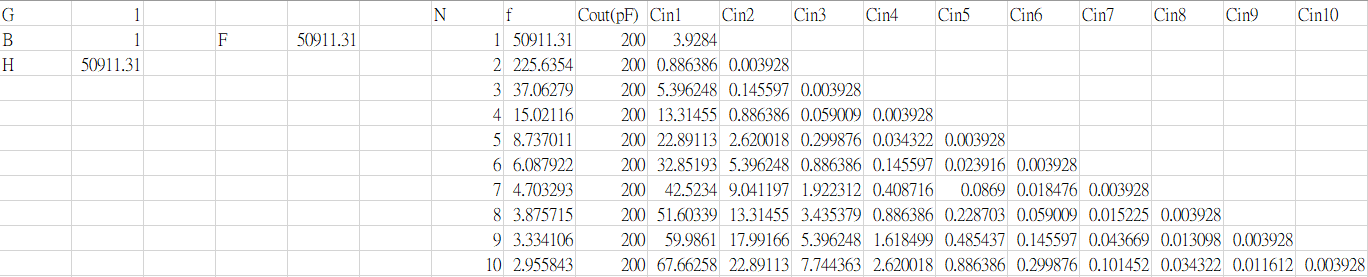
= 20.4093pF

P = CV2f = 43.0441p \* 1.82 \* 50M = 3.3063mW

1.(d)

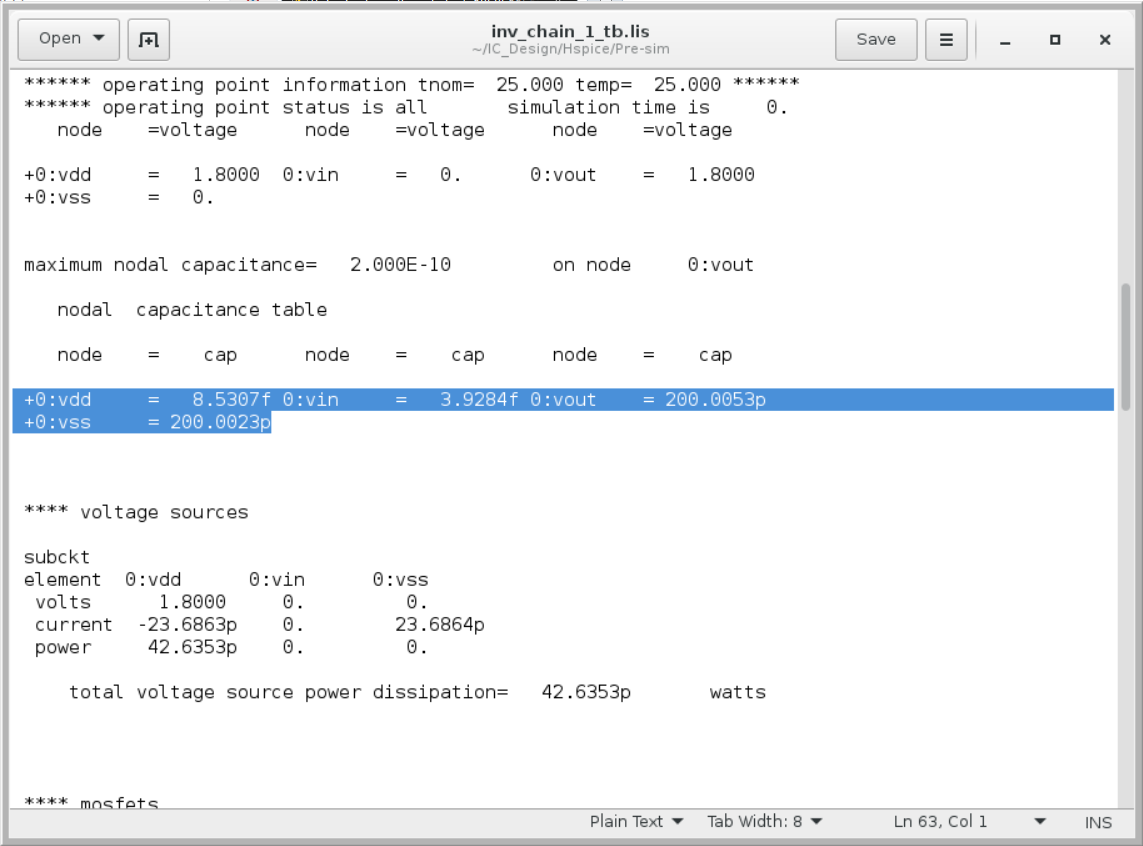
在1(b)的數據圖中，P = 3.4604mW，而(c)我們算得3.3063mW，誤差為4.45%。這可能是因為inverter的 α 不等於 1，因此公式要修正為 αCV2f

2.



2.(1)

N = 1

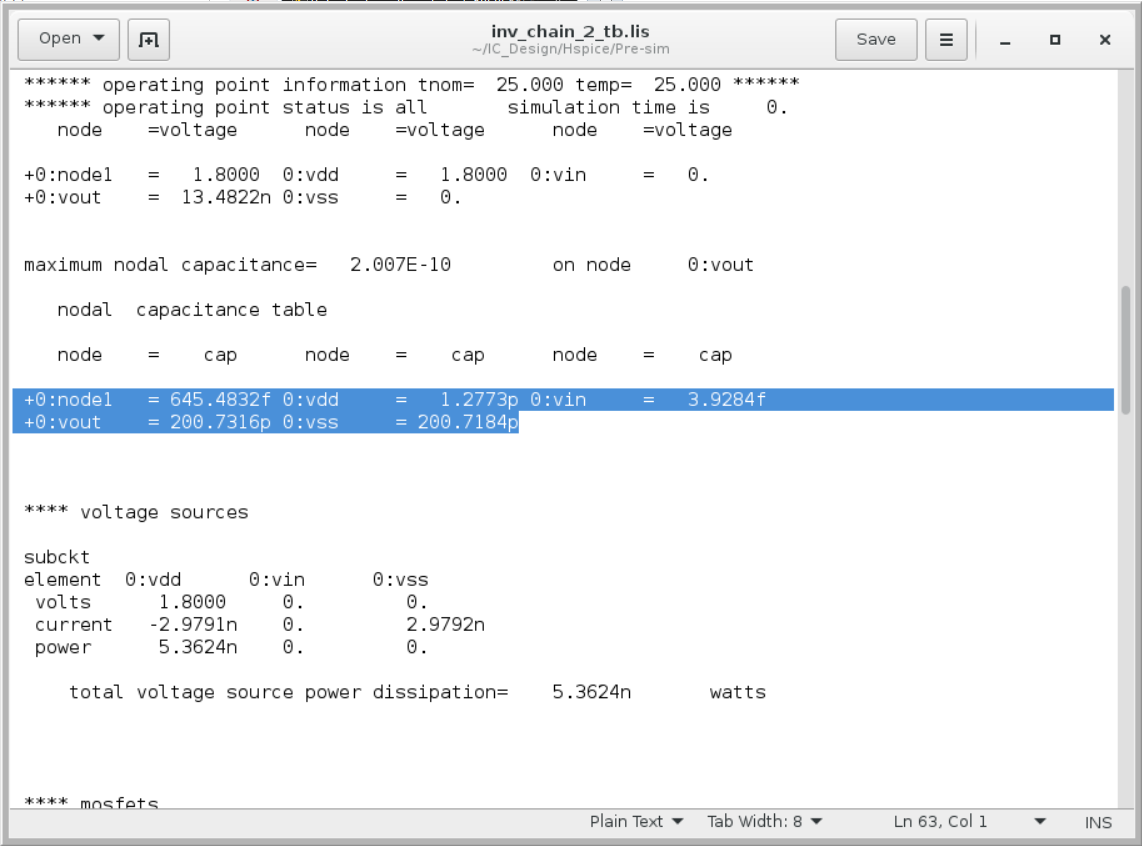


C(total) = Cin + Cout = 3.9284f + 200.0053p

= 200.0092pD

P = CV2f = 200.0092 \* 1.82 \* 50M = 32.4015mW

N = 2



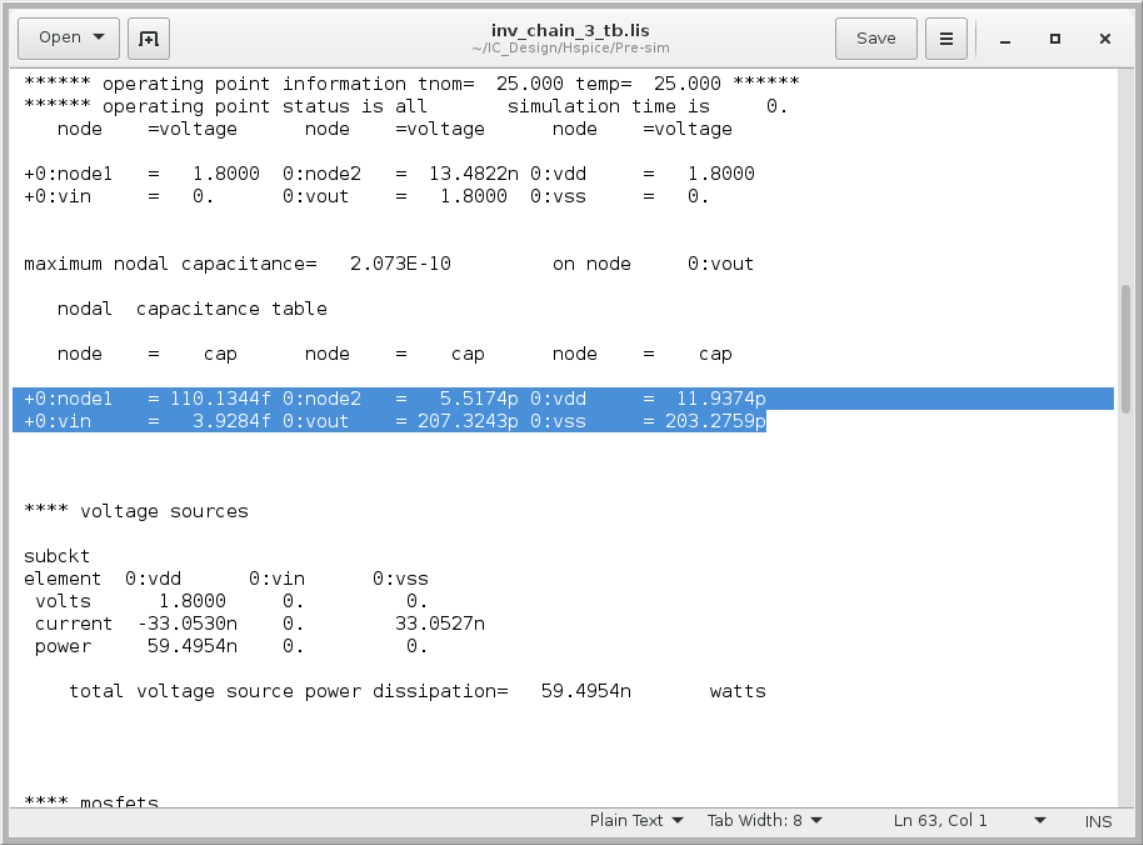
C(total) = Cin + Cout + Cnode1

= 645.4832f + 3.9284f + 200.7316p

= 201.3810pF

P = CV2f = 201.3810p \* 1.82 \* 50M = 32.6237mW

N = 3



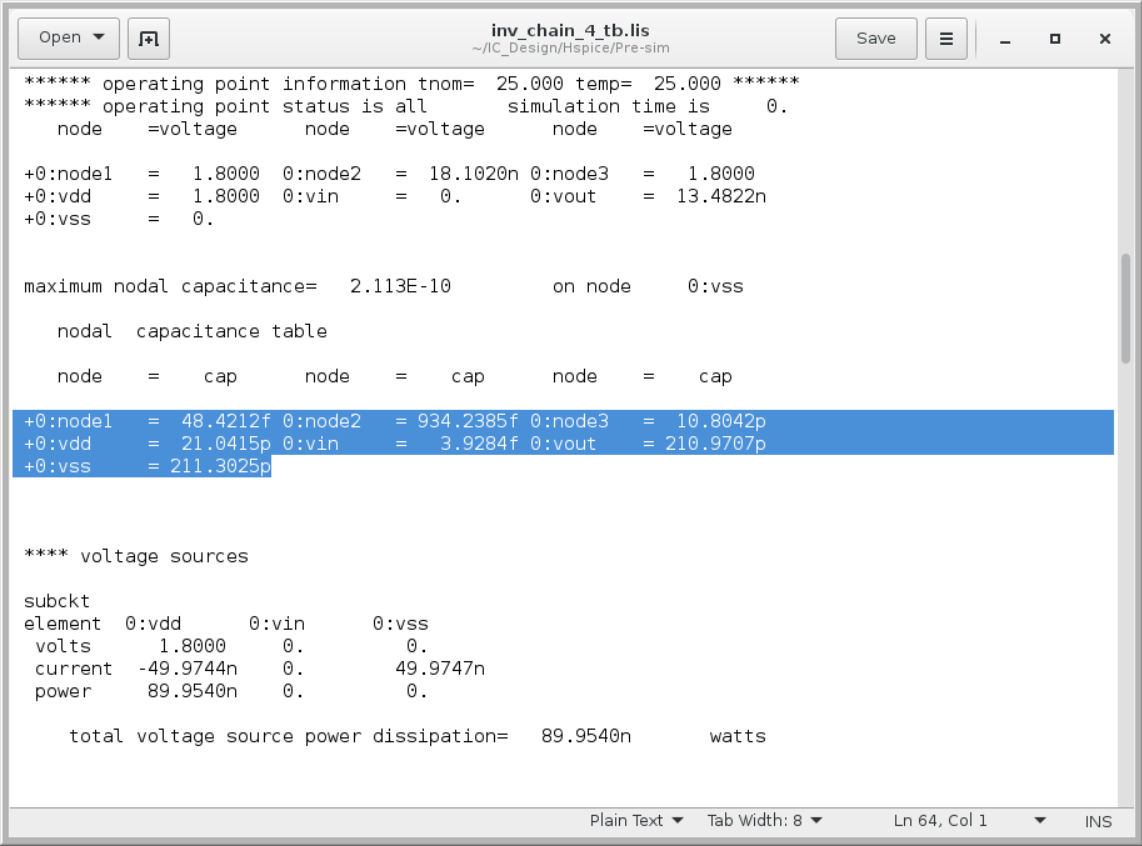
C(total) = Cin + Cout + Cnode1 + Cnode2

= 110.1344f + 5.517p + 3.9284f + 207.3243p

= 212.955pF

P = CV2f = 212.955p \* 1.82 \* 50M = 34.499mW

N = 4



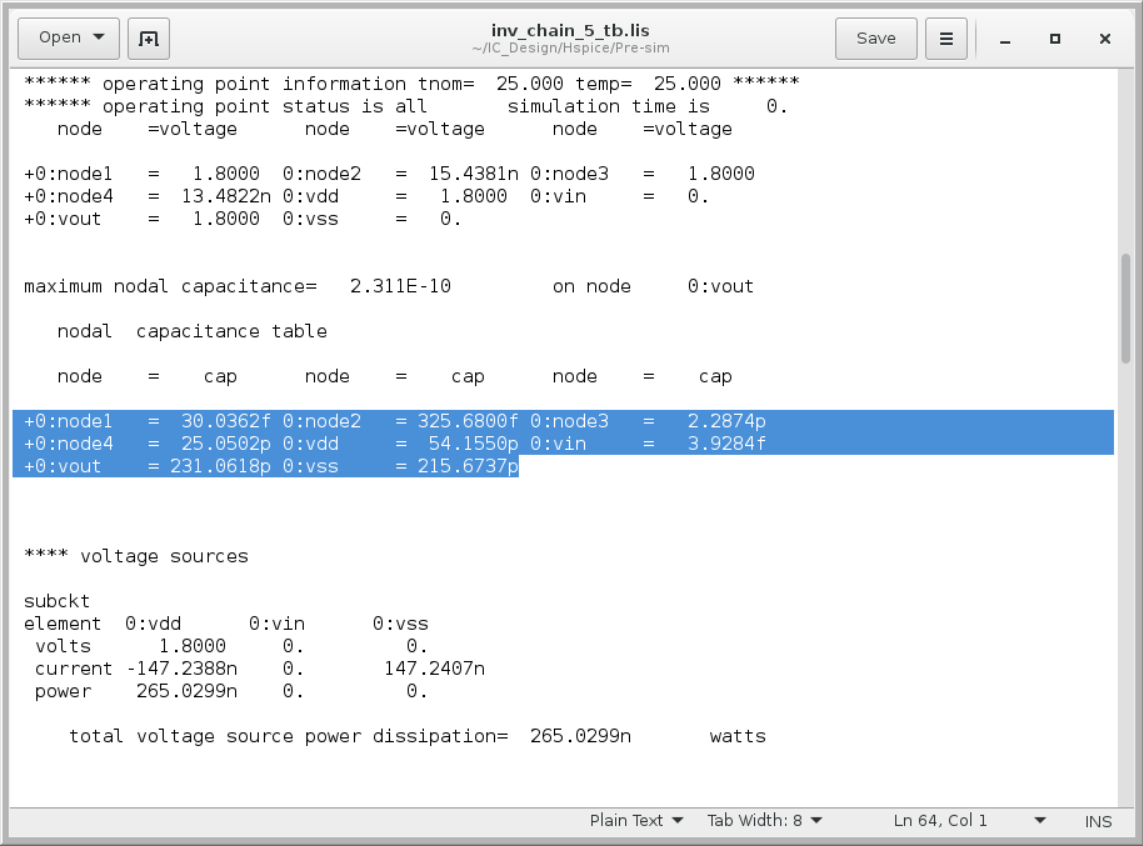
C(total) = Cin + Cout + Cnode1 + … + Cnode3

= 48.4212f + 934.2385f + 10.8042p + 3.9284f + 210.9707p

= 222.7615pF

P = CV2f = 222.76p \* 1.82 \* 50M = 36.0874mW

N = 5



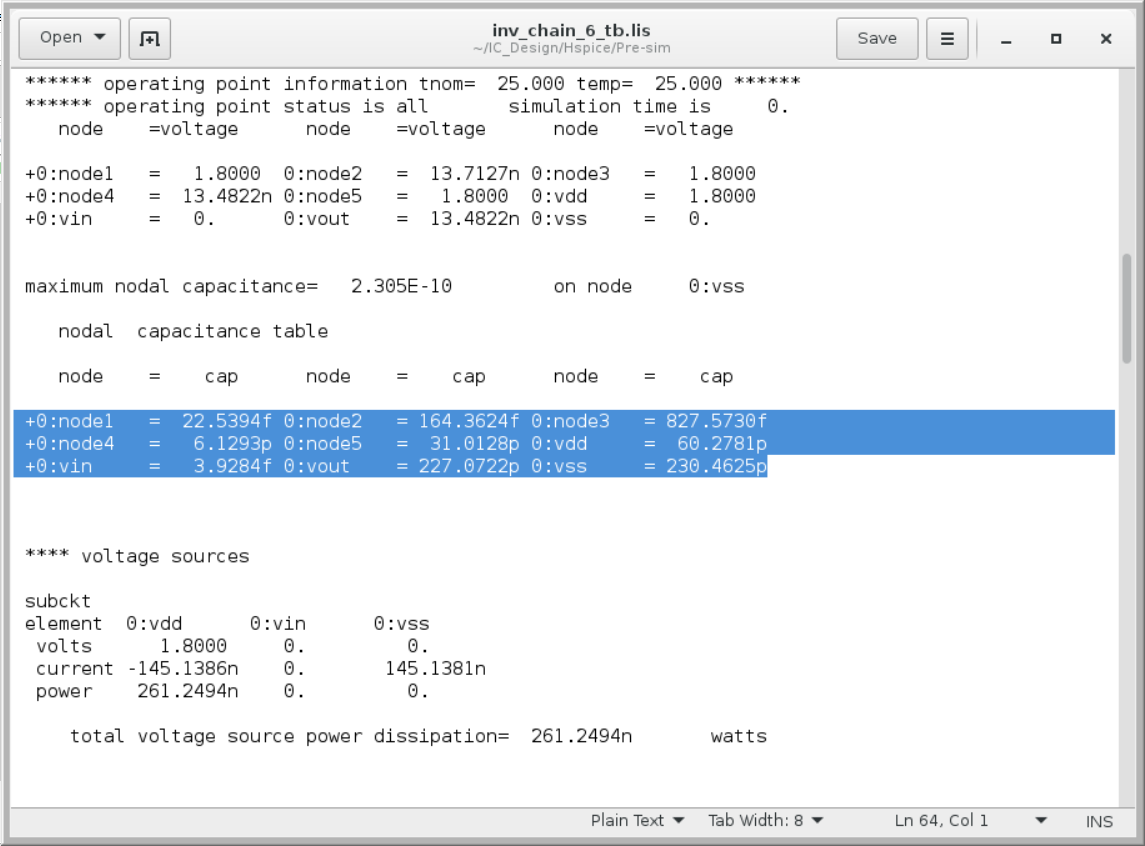
C(total) = Cin + Cout + Cnode1 + … + Cnode4

= 30.0362f + 325.6800f + 2.2874p + 25.0502p + 3.9284f + 215.6737p

= 243.3709pF

P = CV2f = 243.3709pF \* 1.82 \* 50M = 39.3719mW

N = 6



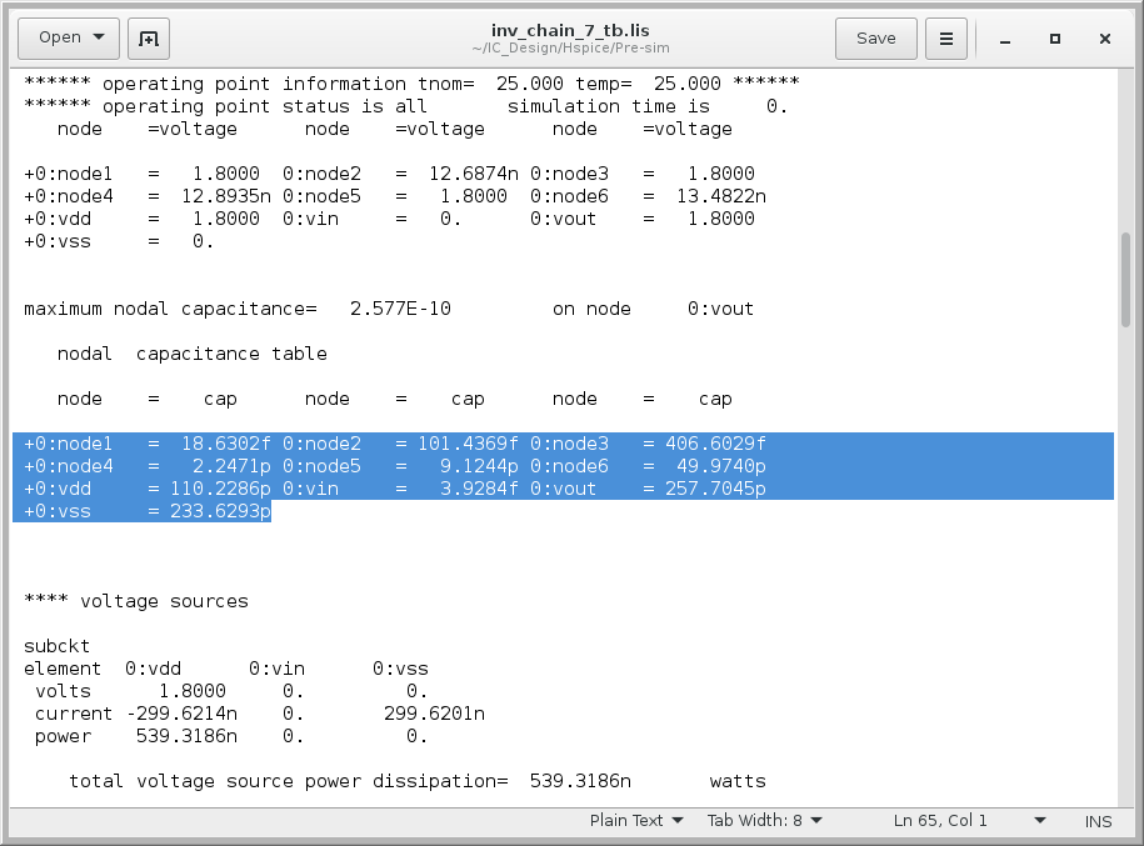
C(total) = Cin + Cout + Cnode1 + … + Cnode5

= 22.5394f + 164.3624f + 827.5730f + 6.1293p + 31.0128p + 3.9284f + 227.0722p

= 265.2327pF

P = CV2f = 265.2327pF \* 1.82 \* 50M = 42.9677mW

N = 7



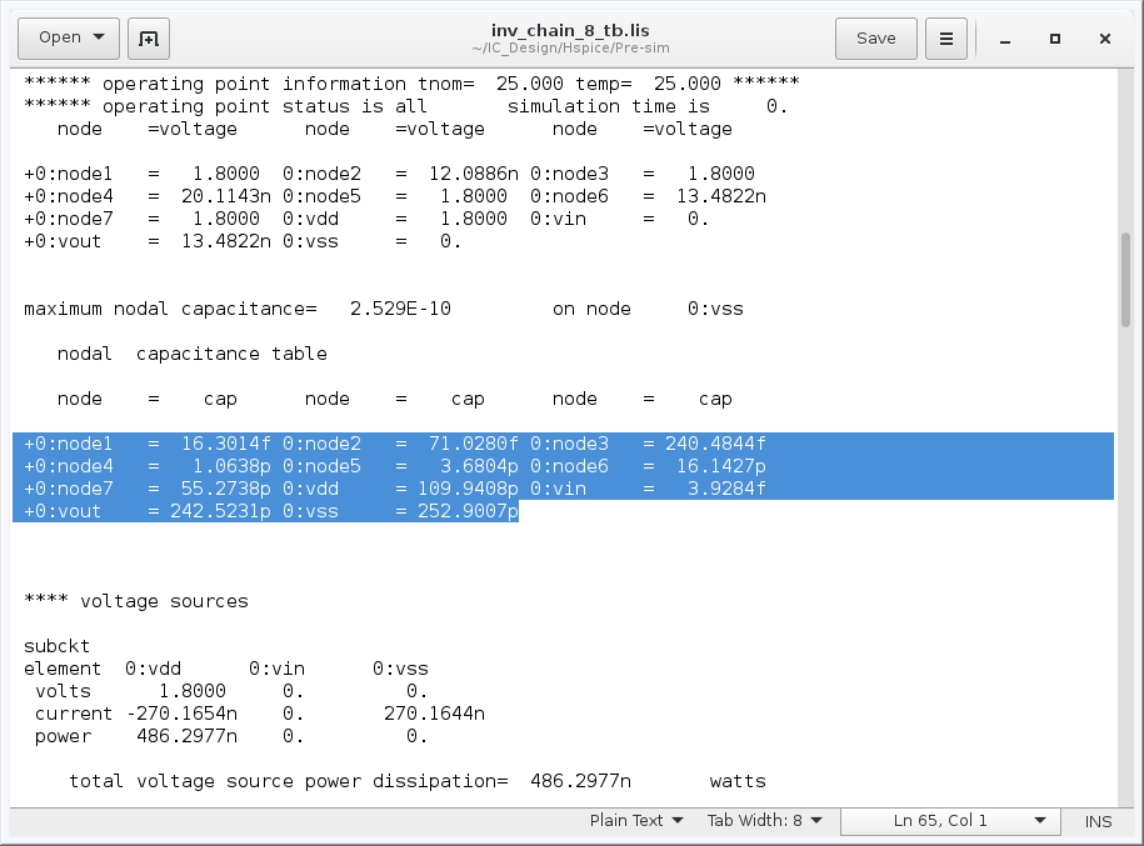
C(total) = Cin + Cout + Cnode1 + … + Cnode6

= 18.6302f + 101.4369f + 406.6029f + 2.2471p + 9.1244p + 49.9740p + 3.9284f + 257.7045p

= 319.5806pF

P = CV2f = 319.5806pF \* 1.82 \* 50M = 51.7721mW

N = 8



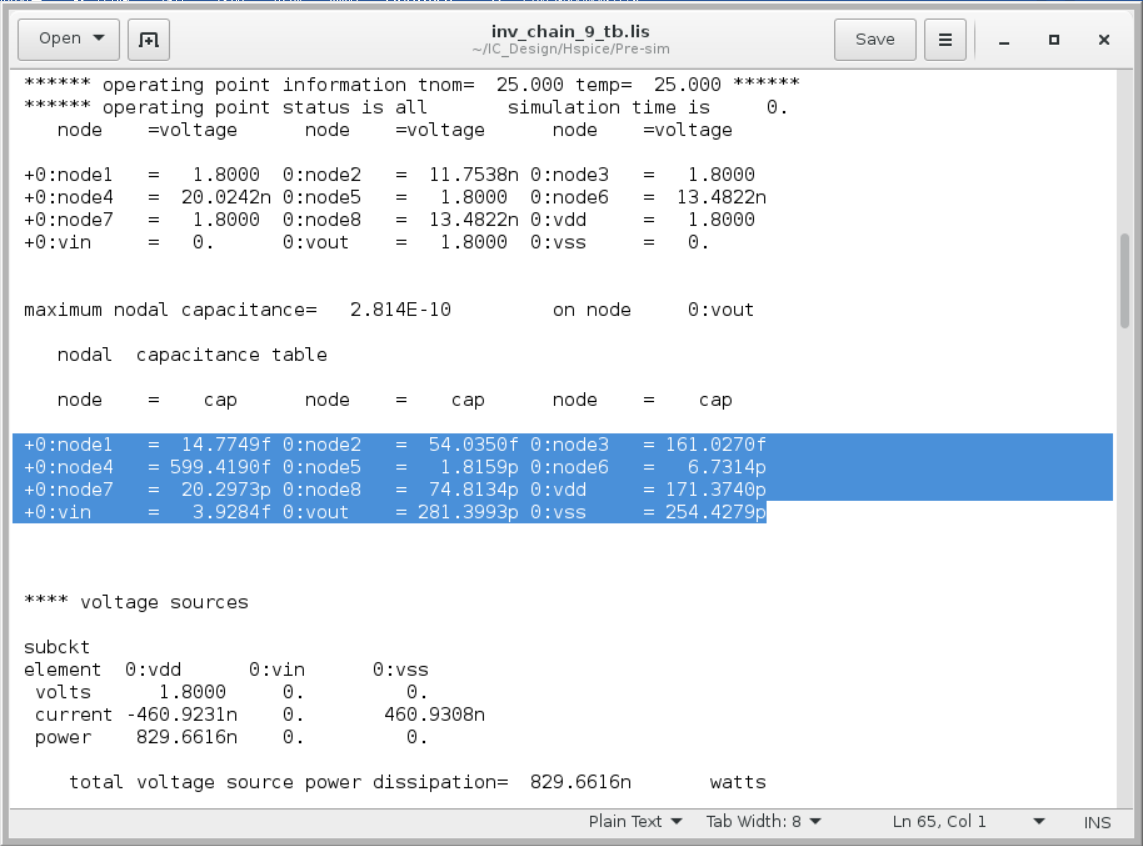
C(total) = Cin + Cout + Cnode1 + … + Cnode7

= 16.3014f + 71.0280f + 240.4844f + 1.0638p + 3.6804p + 16.1427p + 55.2738p + 3.9284f + 242.5231p

= 319.0155pF

P = CV2f = 319.5806pF \* 1.82 \* 50M = 51.6805mW

N = 9



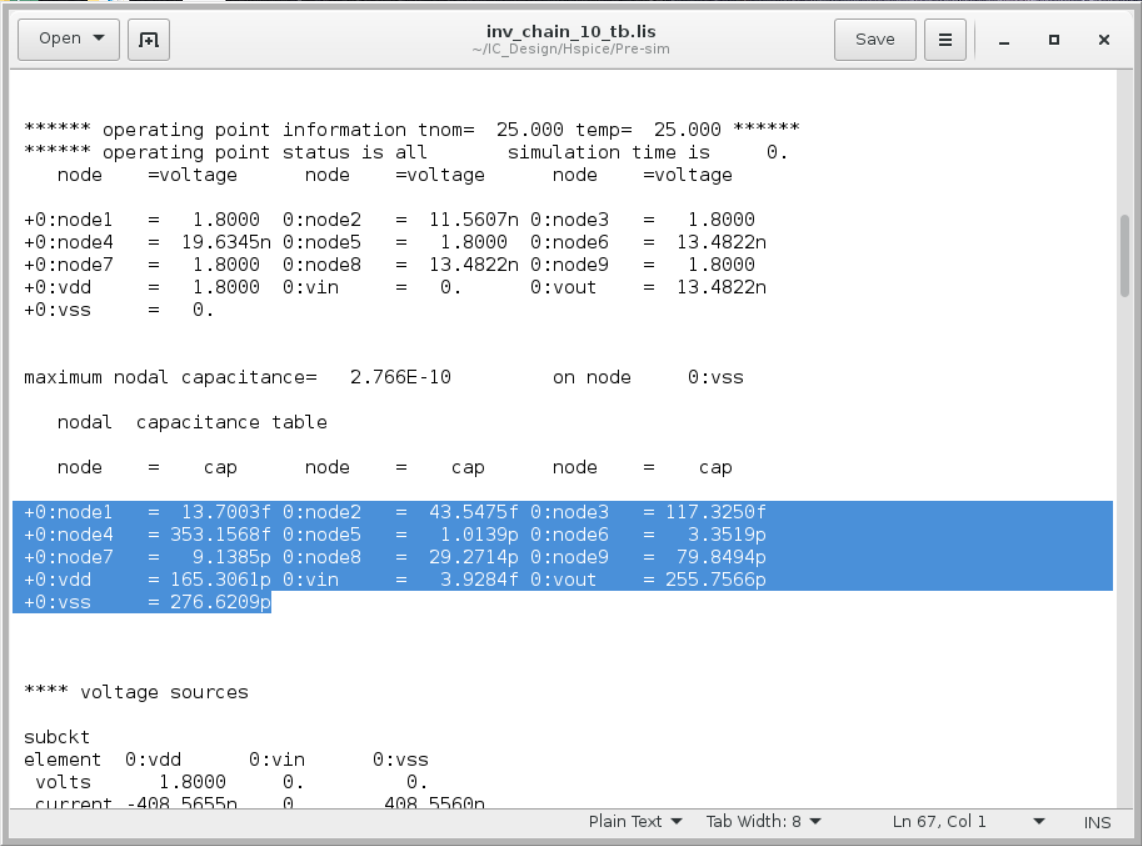
C(total) = Cin + Cout + Cnode1 + … + Cnode8

= 14.7749f + 54.0350f + 161.0270f + 599.4190f + 1.8159p + 6.7314p + 20.2973p + 74.8134p + 3.9284f + 281.3993p

= 385.8905pF

P = CV2f = 385.8905pF \* 1.82 \* 50M = 62.5143mW

N = 10



C(total) = Cin + Cout + Cnode1 + … + Cnode9

= 13.7003f + 43.5475f + 117.3250f + 353.1568f + 1.0139p + 3.3519p + 9.1385p + 29.2714p + 79.8494p + 3.9284f + 255.7566p

= 378.8698pF

P = CV2f = 378.8698pF \* 1.82 \* 50M = 61.377mW

2.(b)

In 1(b), 可得知，when D = 28.49, delay = 454.0129p，因此可推得下表

|  |  |  |  |
| --- | --- | --- | --- |
| N | f | D | delay(ps) |
| 1 | 50911.31249 | 50912.31249 | 811331.9284 |
| 2 | 225.6353529 | 453.2707059 | 7223.262466 |
| 3 | 37.06278905 | 114.1883672 | 1819.690829 |
| 4 | 15.0211635 | 64.08465401 | 1021.244634 |
| 5 | 8.73701052 | 48.6850526 | 775.8386072 |
| 6 | 6.087921571 | 42.52752942 | 677.7131261 |
| 7 | 4.703293078 | 39.92305154 | 636.2085085 |
| 8 | 3.875714579 | 39.00571664 | 621.5899799 |
| 9 | 3.334105715 | 39.00695143 | 621.6096574 |
| 10 | 2.955843453 | 39.55843453 | 630.3980197 |

2.(c)

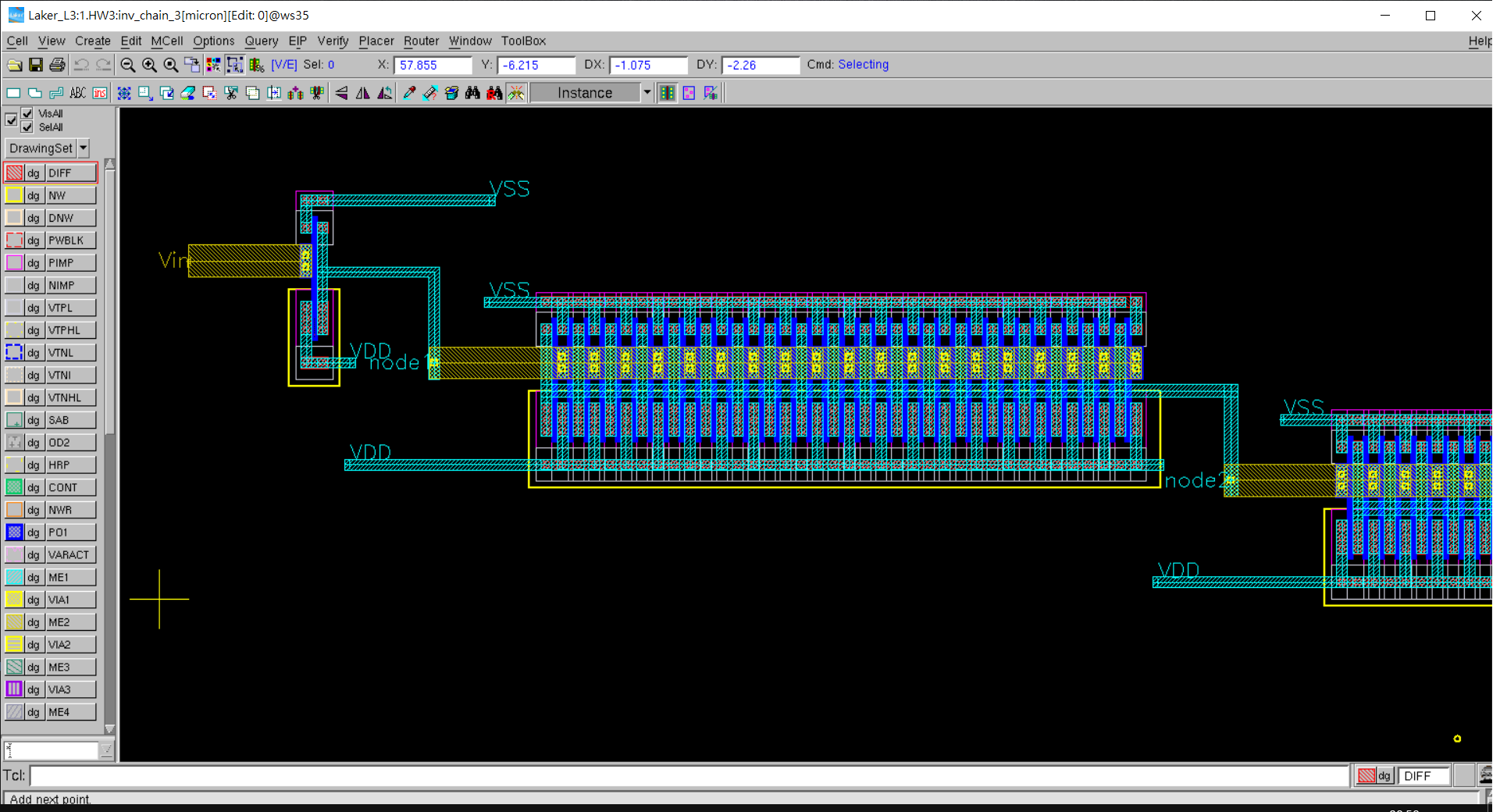
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| N | tpdf | tpdr | power | product |
| 1 | failed | failed | 360.1865u | Not defined |
| 2 | 5.8353n | 5.5720n | 34.1732m | 194.9120f |
| 3 | 1.6348n | 1.6118n | 36.6340m | 59.4680f |
| 4 | 988.5902p | 923.5510p | 39.4466m | 37.7137f |
| 5 | 749.4367p | 752.1306p | 43.8472m | 32.9198f |
| 6 | 667.4663p | 656.5623p | 48.3595m | 32.0147f |
| 7 | 629.8820p | 630.8910p | 53.9929m | 34.0364f |
| 8 | 626.2285p | 607.4136p | 58.9928m | 36.3897f |
| 9 | 622.0113p | 621.3121p | 65.1725m | 40.5152f |
| 10 | 694.6714p | 627.3033p | 70.4994m | 46.5992f |

When N=6, it has minimum “power-delay product”. And it is smaller than the number of stages for the shortest propagation delay, which is N = 8 in Q2b. 這可能是因為在N=5~10時delay都差不多，而power則是隨著N慢慢上升，兩者平衡之下N=6便為最佳解。

2.(d)

一張含有 螢幕擷取畫面, 電子用品, 電腦, 監視器 的圖片

自動產生的描述



Layout

一張含有 螢幕擷取畫面 的圖片

自動產生的描述

DRC

一張含有 螢幕擷取畫面 的圖片

自動產生的描述

LVS

一張含有 文字, 地圖 的圖片

自動產生的描述

我有將inverter翻轉再合併，以共用metal, contact, and Diffusion；共用Diffusion可以降低delay

一張含有 螢幕擷取畫面 的圖片

自動產生的描述in2(c), power = 59.4680f, tpdf = 1.6348n, tpdr = 1.6118n

At here, power = 17.8572, tpdf = 3.5468n, tpdr = 8.9746n

我們可以觀察到power減少為1/3，但delay卻放大很多倍。我覺得主要跟我的layout方式有關，有可能我這樣layout讓許多MOS不用因此開開關關，讓 α 降低。但也因此要等其他MOS處理完才能運算，所以delay也增加許多